Fig 1

Figure 2
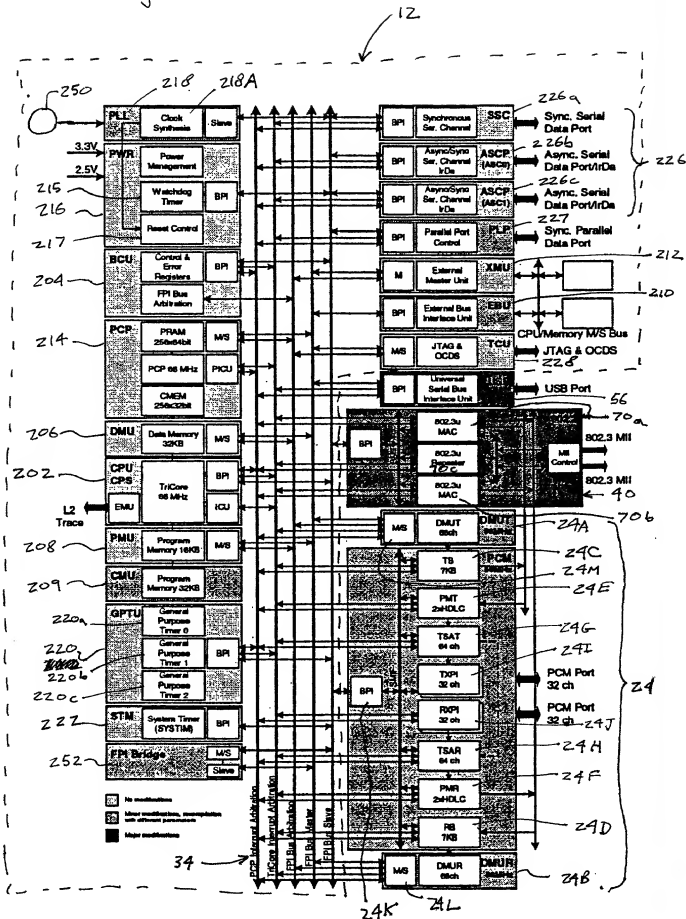

Figure 2

HARRIER: C10-Architecture

Infineon technologies
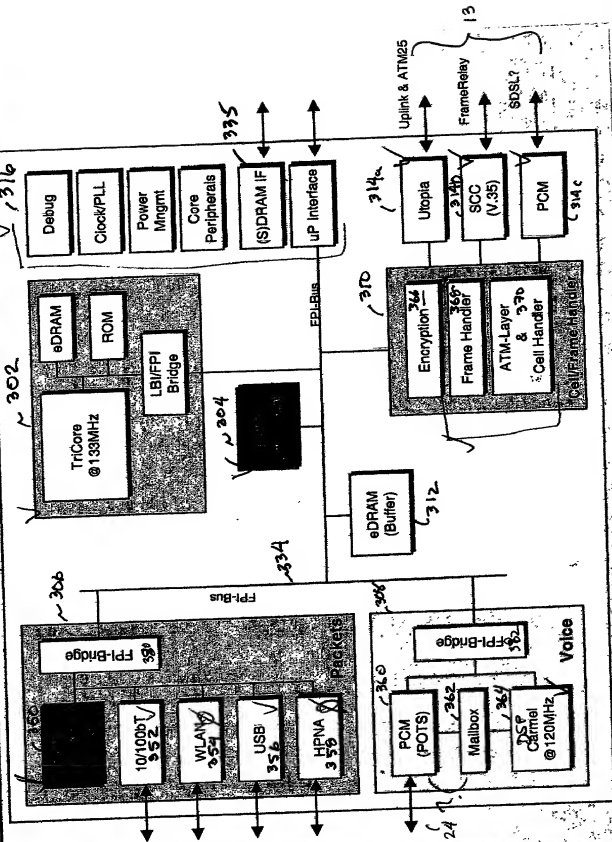
Fig. 3

Debug | Clock/PLL | Power Mngmt | Core Peripherals | (S)DRAM IF | uP Interface

eDRAM | ROM

TriCore @133MHz

LBI/FPI Bridge

FPI-Bus

Utopia | SCC (V.35) | PCM

Encryption | Frame Handler | ATM-Layer & Cell Handler

Cell/Frame Handler

Uplink & ATM25

FrameRelay

SDSL2

eDRAM (Buffer)

FPI-Bus

FPI-Bridge

10/100bT | WLAN | USB | HPNA

Packets

FPI-Bridge

PCM (POTS) | Mailbox | DSP Carmel @120MHz

Voice